

features

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval†
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Using Human Body Model (C = 100 pF, R = 1500 Ω)
- Power-On Reset Generator With Fixed Delay Time of 200 ms (TPS3823/4/5/8) or 25 ms (TPS3820)
- Manual Reset Input (TPS3820/3/5/8)
- Reset Output Available in Active-Low (TPS3820/3/4/5), Active-High (TPS3824) and Open-Drain (TPS3828)
- Supply Voltage Supervision Range 2.5 V, 3 V, 3.3 V, 5 V
- Watchdog Timer (TPS3820/3/4/8)
- Supply Current of 15 μA (Typ)
- SOT23-5 Package

applications

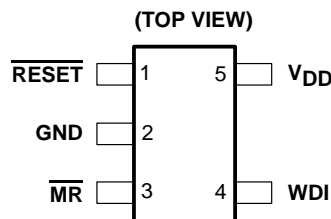
- Applications Using Automotive DSPs, Microcontrollers, or Microprocessors
- Industrial Equipment
- Programmable Controls
- Automotive Systems
- Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communications Systems

† Contact factory for details. Q100 qualification data available on request.

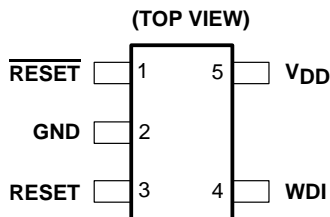
description

The TPS382x family of supervisors provides circuit initialization and timing supervision, primarily for DSP and processor-based systems.

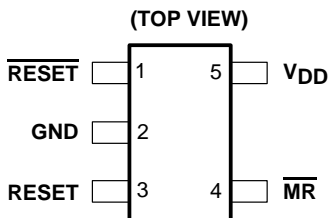
TPS3820, TPS3823, TPS3828 . . . DBV PACKAGE



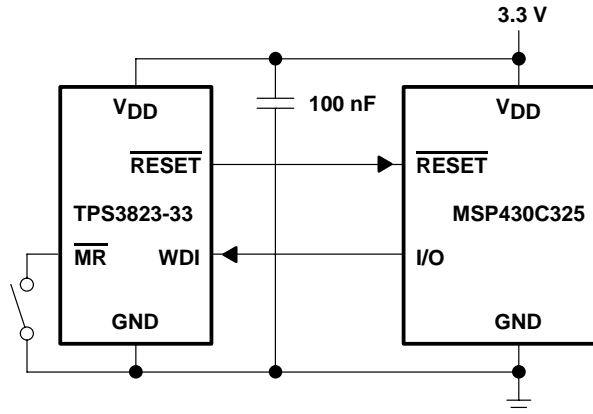
TPS3824 . . . DBV PACKAGE



TPS3825 . . . DBV PACKAGE



typical application



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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description (continued)

During power-on, $\overline{\text{RESET}}$ is asserted when supply voltage V_{DD} becomes higher than 1.1 V. Thereafter, the supply voltage supervisor monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage $V_{\text{IT-}}$. An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_{d} , starts after V_{DD} has risen above the threshold voltage $V_{\text{IT-}}$. When the supply voltage drops below the threshold voltage $V_{\text{IT-}}$, the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage $V_{\text{IT-}}$ set by an internal voltage divider.

The TPS3820/3/5/8 devices incorporate a manual reset input, $\overline{\text{MR}}$. A low level at $\overline{\text{MR}}$ causes $\overline{\text{RESET}}$ to become active. The TPS3824/5 devices include a high-level output RESET. TPS3820/3/4/8 have a watchdog timer that is periodically triggered by a positive or negative transition at WDI. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, t_{tout} , $\overline{\text{RESET}}$ becomes active for the time period t_{d} . This event also reinitializes the watchdog timer. Leaving WDI unconnected disables the watchdog.

In applications where the input to the WDI pin may be active (transitioning high and low) when the TPS3820/3/4/8 is asserting $\overline{\text{RESET}}$, the TPS3820/3/4/8 does not return to a non-reset state when the input voltage is above V_{t} . If the application requires that input to WDI is active when $\overline{\text{RESET}}$ is asserted, WDI must be decoupled from the active signal. This can be accomplished by using an N-channel FET in series with the WDI pin, with the gate of the FET connected to the $\overline{\text{RESET}}$ output as shown in Figure 1.

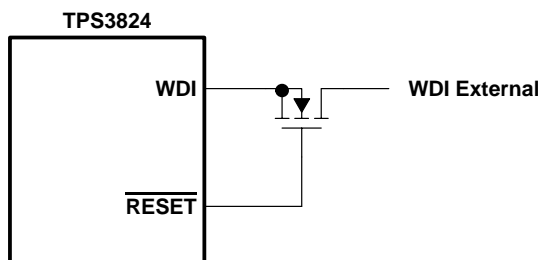


Figure 1

The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 5-pin SOT23-5 package. The TPS382x-xxQ-Q1 devices are characterized for operation over a temperature range of -40°C to 125°C , and are qualified in accordance with AEC-Q100 stress test qualification for integrated circuits.

TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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PACKAGE INFORMATION

DEVICE NAME	THRESHOLD VOLTAGE	MARKING
TPS3820-33QDBVRQ1†	2.93 V	PDEQ
TPS3820-50QDBVRQ1†	4.55 V	PDDQ
TPS3823-25QDBVRQ1†	2.25 V	PAPQ
TPS3823-30QDBVRQ1†	2.63 V	PAQQ
TPS3823-33QDBVRQ1†	2.93 V	PARQ
TPS3823-50QDBVRQ1†	4.55 V	PASQ
TPS3824-25QDBVRQ1†	2.25 V	PATQ
TPS3824-30QDBVRQ1†	2.63 V	PAUQ
TPS3824-33QDBVRQ1†	2.93 V	PAVQ
TPS3824-50QDBVRQ1†	4.55 V	PAWQ
TPS3825-33QDBVRQ1†	2.93 V	PDGQ
TPS3825-50QDBVRQ1†	4.55 V	PDFQ
TPS3828-33QDBVRQ1†	2.93 V	PDIQ
TPS3828-50QDBVRQ1†	4.55 V	PDHQ

† The DBVR package indicates tape and reel of 3000 parts.

FUNCTION/TRUTH TABLE

INPUTS		OUTPUTS	
\overline{MR}^\ddagger	$V_{DD} > V_{IT}$	\overline{RESET}	$RESET^\S$
L	0	L	H
L	1	L	H
H	0	L	H
H	1	H	L

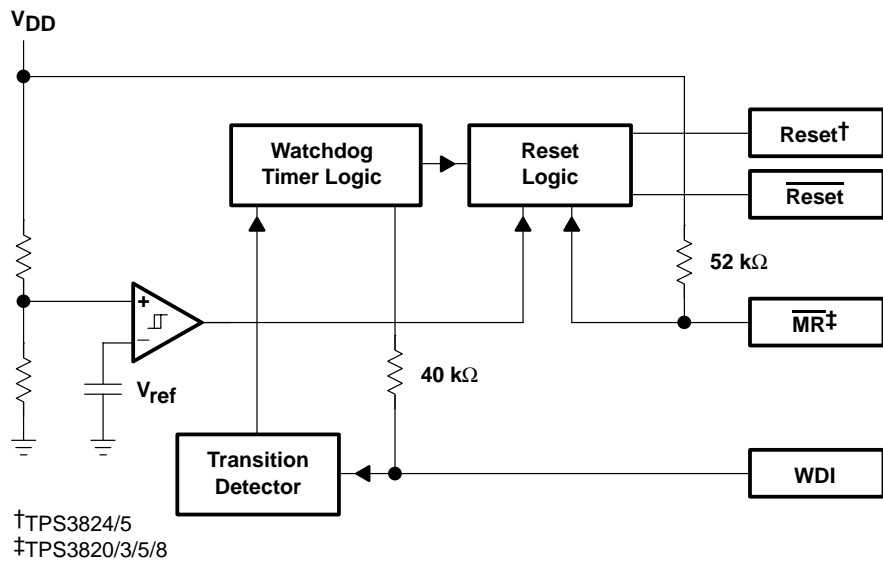
‡ TPS3820/3/5/8

§ TPS3824/5

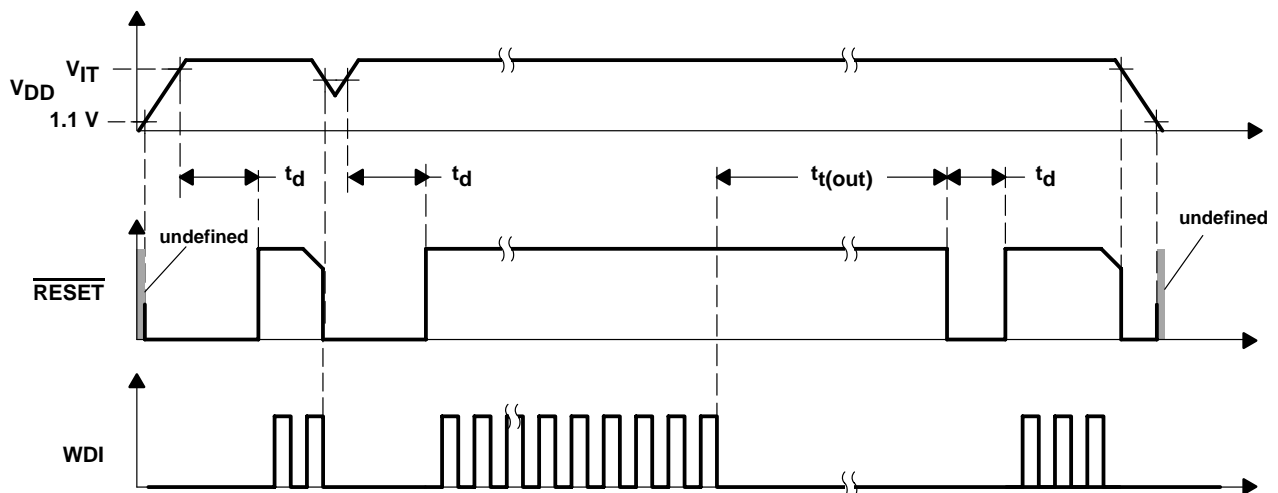
TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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functional block diagram



timing diagram



TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	6 V
RESET, $\overline{\text{RESET}}$, MR, WDI (see Note 1)	-0.3 V to ($V_{DD} + 0.3$ V)
Maximum low output current, I_{OL}	5 mA
Maximum high output current, I_{OH}	-5 mA
Input clamp current range, I_{IK} ($V_I < 0$ or $V_I > V_{DD}$)	± 10 mA
Output clamp current range, I_{OK} ($V_O < 0$ or $V_O > V_{DD}$)	± 10 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-40°C to 125°C
Storage temperature range, T_{stg}	-65°C to 150°C
Soldering temperature	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW	87 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.1	5.5	V
Input voltage, V_I	0	$V_{DD} + 0.3$	V
High-level input voltage at $\overline{\text{MR}}$ and WDI, V_{IH}	$0.7 \times V_{DD}$		V
Low-level input voltage, V_{IL}		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\overline{\text{MR}}$ or WDI, $\Delta t/\Delta V$		100	ns/V
Operating free-air temperature range, T_A	-40	125	°C



TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
V _{OH}	High-level output voltage	RESET	TPS382x-25	0.8 × V _{DD}		V		
			TPS382x-30					
			TPS382x-33					
				TPS382x-50	V _{DD} – 1.5 V			
		RESET	TPS3824-25	V _{DD} ≥ 1.8 V, I _{OH} = –100 μA	0.8 × V _{DD}		V	
	TPS3825-25							
	TPS3824-30							
	TPS3825-30							
			TPS3824-33	V _{DD} ≥ 1.8 V, I _{OH} = –150 μA				
			TPS3825-33					
			TPS3824-50					
			TPS3825-50					
V _{OL}	Low-level output voltage	RESET	TPS3824-25			0.4	V	
			TPS3825-25					
			TPS3824-30					
			TPS3825-30					
					TPS3824-33	V _{DD} = V _{IT–} + 0.2 V		
					TPS3825-33			
					TPS3824-50	V _{DD} = V _{IT–} + 0.2 V		
					TPS3825-50			
	RESET	TPS382x-25	V _{DD} = V _{IT–} – 0.2 V			0.45	V	
			TPS382x-30	V _{DD} = V _{IT–} – 0.2 V				
			TPS382x-33					
			TPS382x-50	V _{DD} = V _{IT–} – 0.2 V				
Power-up reset voltage (see Note 2)			V _{DD} ≥ 1.1 V, I _{OL} = 20 μA			0.4	V	
V _{IT–}	Negative-going input threshold voltage (see Note 3)	T _A = 0°C to 85°C	TPS382x-25		2.21	2.25	2.30	V
			TPS382x-30		2.59	2.63	2.69	
			TPS382x-33		2.88	2.93	3	
			TPS382x-50		4.49	4.55	4.64	
		T _A = –40°C to 125°C	TPS382x-25		2.19	2.25	2.30	V
			TPS382x-30		2.55	2.63	2.69	
			TPS382x-33		2.84	2.93	3	
			TPS382x-50		4.44	4.55	4.65	
V _{hys}	Hysteresis at V _{DD} input	TPS382x-25				30	mV	
		TPS382x-30						
		TPS382x-33						
		TPS382x-50						50

NOTES: 2. The lowest supply voltage at which RESET becomes active. t_r, V_{DD} ≥ 15 μs/V
 3. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 μF) should be placed near the supply terminals.



TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH(AV)}$	Average high-level input current	WDI WDI = V_{DD} , time average (dc = 88%)		120		μA
$I_{IL(AV)}$	Average low-level input current		WDI = 0.3 V, $V_{DD} = 5.5$ V time average (dc = 12%)	-15		
I_{IH}	High-level input current	WDI	WDI = V_{DD}	140	190	
		\overline{MR}	$\overline{MR} = V_{DD} \times 0.7$, $V_{DD} = 5.5$ V	-40	-60	
I_{IL}	Low-level input current	WDI	WDI = 0.3 V, $V_{DD} = 5.5$ V	140	190	
		\overline{MR}	$\overline{MR} = 0.3$ V, $V_{DD} = 5.5$ V	-110	-160	
I_{OS}	Output short-circuit current (see Note 4)	\overline{RESET}	TPS382x-25	$V_{DD} = V_{IT, max} + 0.2$ V, $V_O = 0$ V	-400	μA
			TPS382x-30			
			TPS382x-33			
			TPS382x-50			
I_{DD}	Supply current	WDI and \overline{MR} unconnected, Outputs unconnected		15	25	μA
	Internal pullup resistor at \overline{MR}			52		k Ω
C_i	Input capacitance at \overline{MR} , WDI	$V_I = 0$ V to 5.5 V		5		pF

NOTE 4: The \overline{RESET} short-circuit current is the maximum pullup current when \overline{RESET} is driven low by a μP bidirectional reset pin.

timing requirements at $R_L = 1$ M Ω , $C_L = 50$ pF, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT	
t_w	Pulse width	at V_{DD}	$V_{DD} = V_{IT-} + 0.2$ V, $V_{DD} = V_{IT-} - 0.2$ V	6		μs
		at \overline{MR}	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	1		μs
		at WDI	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$	100		ns

switching characteristics at $R_L = 1$ M Ω , $C_L = 50$ pF, $T_A = 25^\circ C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{tout}	Watchdog time out	TPS3820	$V_{DD} \geq V_{IT-} + 0.2$ V,	112	200	310	ms
		TPS3823/4/8	See Timing Diagram	0.9	1.6	2.5	s
t_d	Delay time	TPS3820	$V_{DD} \geq V_{IT-} + 0.2$ V,	15	25	37	ms
		TPS3823/4/5/8	See timing diagram	120	200	300	
t_{PHL}	Propagation (delay) time, high-to-low-level output	\overline{MR} to \overline{RESET} delay (TPS3820/3/5/8)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.1	μs
		V_{DD} to \overline{RESET} delay	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			25	
t_{PLH}	Propagation (delay) time, low-to-high-level output	\overline{MR} to \overline{RESET} delay (TPS3824/5)	$V_{DD} \geq V_{IT-} + 0.2$ V, $V_{IL} = 0.3 \times V_{DD}$, $V_{IH} = 0.7 \times V_{DD}$			0.1	μs
		V_{DD} to \overline{RESET} delay (TPS3824/5)	$V_{IL} = V_{IT-} - 0.2$ V, $V_{IH} = V_{IT-} + 0.2$ V			25	



TYPICAL CHARACTERISTICS

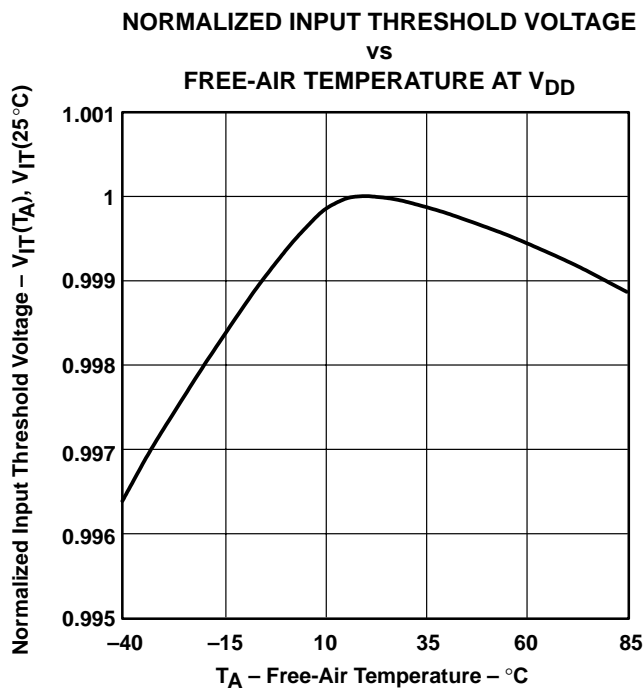


Figure 2

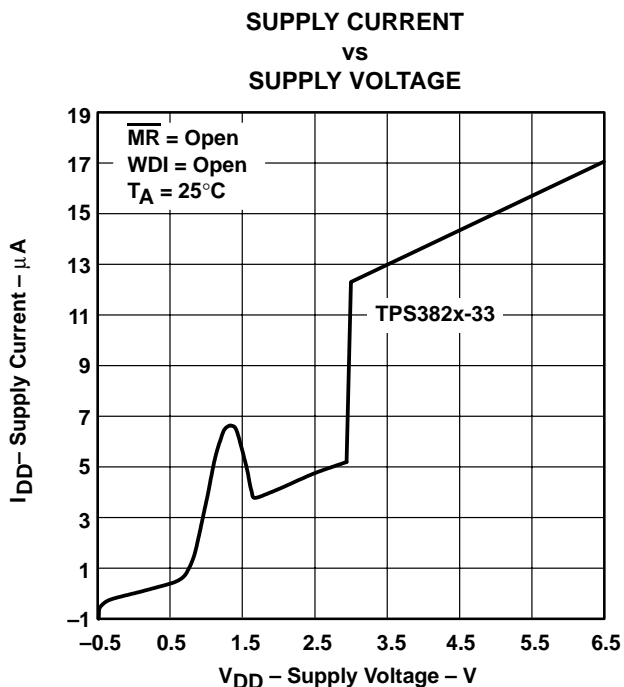


Figure 3

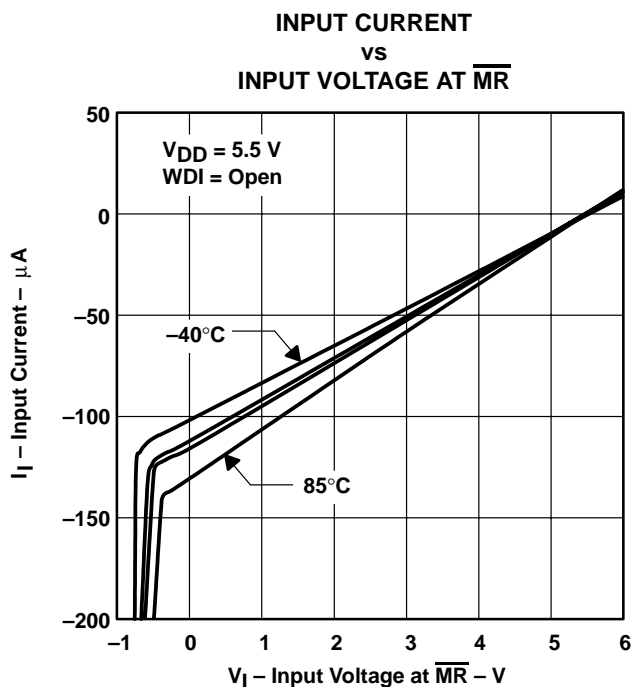


Figure 4

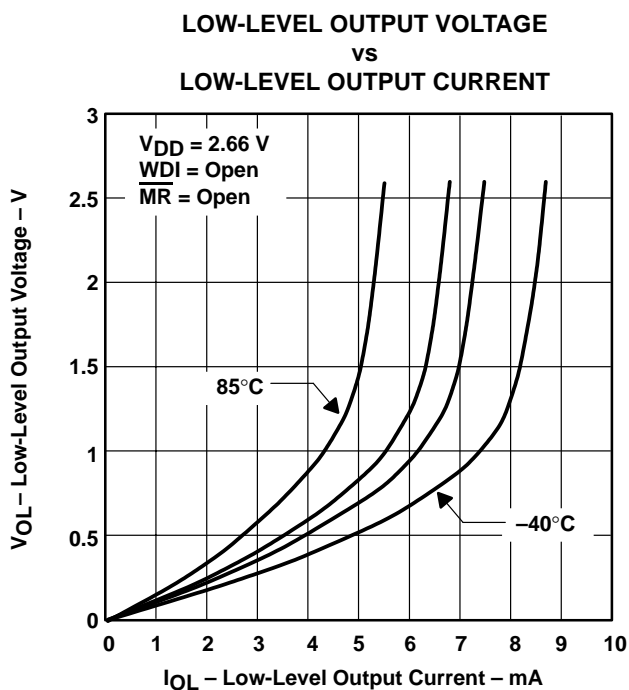


Figure 5

TYPICAL CHARACTERISTICS

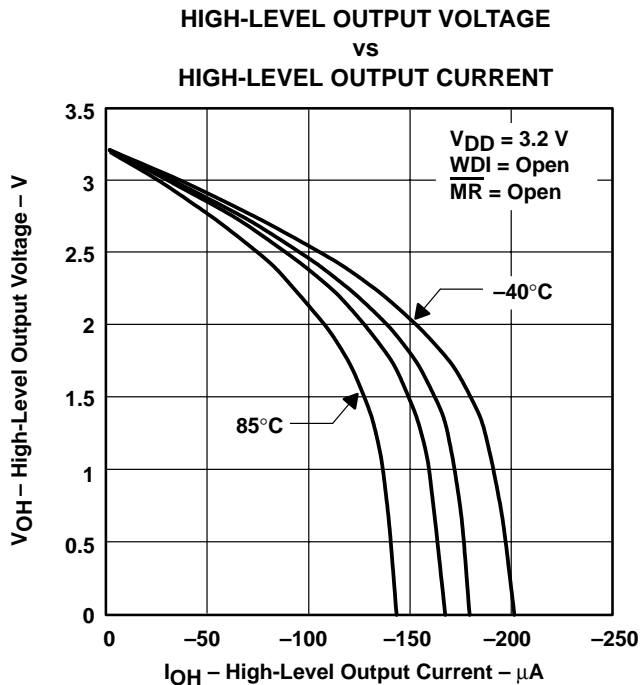


Figure 6

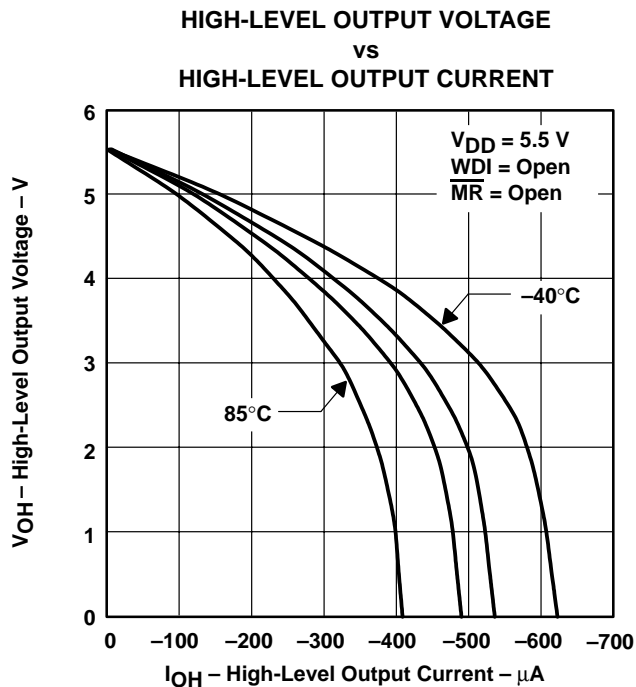


Figure 7

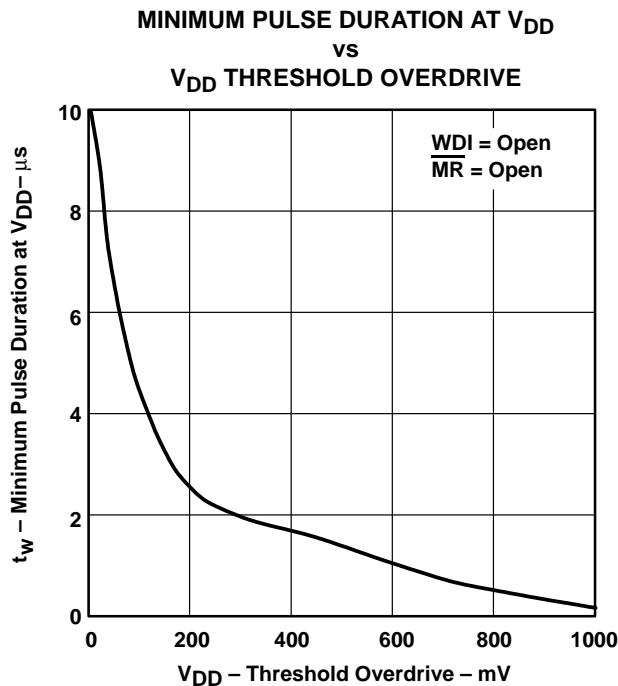


Figure 8

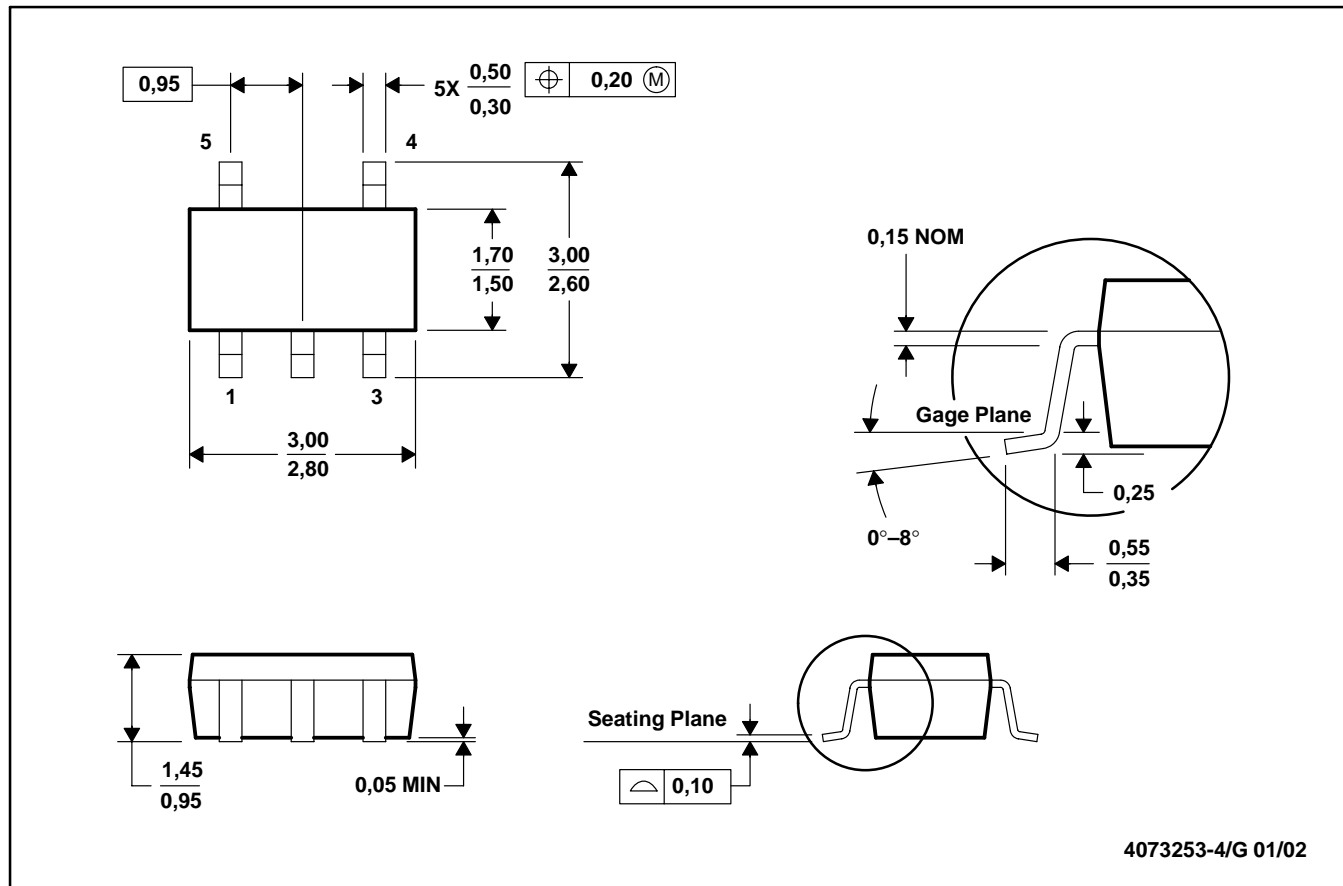
TPS3820-xx-Q1, TPS3823-xx-Q1, TPS3824-xx-Q1, TPS3825-xx-Q1, TPS3828-xx-Q1 PROCESSOR SUPERVISORY CIRCUITS

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MECHANICAL DATA

DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-178

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS3820-33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3820-50DBVRQ1G4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3820-50QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3823-25QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3823-30QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3823-33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3823-50QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3824-25QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3824-30QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3824-33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3824-50QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3825-33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3825-50QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM
TPS3828-33QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3828-50QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	TBD	CU NIPDAU	Level-1-220C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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